REMARKS

The undersigned, a pro-se applicant, respectfully requests that if the Examiner finds patentable subject matter disclosed in this application, but feels that Applicant's present claim is not entirely suitable, the Examiner draft one or more allowable claims for applicant.

This case has been carefully reviewed and analyzed in view of the Official Action dated December 21, 2001.

The Examiner has objected to the drawings because of informalities. The feature has been canceled from the new claim in order to avoid this objection.

Further, the Examiner has objected to claim 1 because of informalities. Claims 1-4 have been canceled and replaced with new claim 5 in order to avoid this objection.

Furthermore, the Examiner has rejected claims 1-4 under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it si most nearly connected, to make and/or use the invention. Claims 1-4 have been canceled and replaced with new claim 5 in order to avoid this rejection.

Moreover, the Examiner has r Claims 1-4 have been canceled and replaced with new claim 5 in order to avoid this objection. Claims 1-4 have been canceled and replaced with new claim 5 in order to avoid this rejection. However, if the new claim 5 still does not comply with the requirement, an Examiner's amendment is earnestly solicited.

U.S.C. 102(b) as being anticipated by Hiruta et al (US 5,461,197). Further, the Examiner has rejected claims 2 and 4 under 35 U.S.C. 103(a) as being unpatentable over Hiruta. However, it is respectfully requested that this rejection be withdrawn in light of the following reasons.

Hiruta et al discloses an electronic device comprising a semiconductor chip having an external bump terminal, a board having a via hole whose position corresponds to that of the external bump terminal of said semiconductor chip, a size of the via hole being equal to or larger than the external bump terminal of the semiconductor chip, the board also having an external bump terminal on one surface of the said board, a size of the external bump terminal of said board being larger than the size of the via hole, said board mounting said semiconductor chip thereon in a state that the external bump terminal of said board is connected to the external bump terminal of said semiconductor chip through the via hole, and an envelope of sealing at least a gap between said semiconductor chip and said board. Nevertheless, this reference fails to disclose an ultra-thin film package, wherein polymeric film die carrier or polyimide (PI) die carrier is employed, and the leg position for die bonding is made into a recess shape to lower the thickness after bonding, and polymeric film die carrier or PI die carrier is made into a thin film shape by a fabrication technique, and the I/O leg position is made into a recess shape and the die is glued to the polymeric film die carrier or PI die carrier and then changed with a package material, and by means of a dicing step, a single package granule containing dies is cut, wherein polymeric film die carrier or PI die carrier and the die are soldered at one end of a wire, the other end is mounted with a metal pad within the leg position which is recessed on the polymeric die film carrier or PI die carrier, and the electrode of the metal pad is protruded from the back face of the polymeric film die carrier or PI die carrier, a metal plate is provided at the polymeric film die carrier or PI die carrier, corresponding to the back face of the die position, the electrical bonding of the die with polymeric film die carrier or PI die carrier is a die bonding method such that the I/O bump of the die and the metal pad on the leg position of the polymeric film die carrier or PI die carrier are bonded. Hence, this reference can be clearly

distinguished from the present invention in structure.

Accordingly, the disclosure of the cited reference still fails to teach each and every element of the claimed invention and so the subject matter sought to be patented as a whole would not have been obvious to one of ordinary skill in the art.

The applicant has reviewed the prior art as cited by the Examiner but not used in the rejection and believes that the new claim as presently claimed clearly and distinctly patentably defines over such prior art.

It is now believed that the subject Patent Application has been placed in condition of allowance, and such action is respectfully requested.

Respectfully submitted,

Mary S. Duh

Signature

Mary S. Duh

President

For: ORIENT SEMICONDUCTOR ELECTRONICS LIMITED (ASSIGNEE OF RECORD)

RECORDATION DATE: 04/16/2001

REEL/FRAME 011719/0835

Date: April 22, 2002